Course Name : Computer Organization

Course Code	Course Type	Regular Semester	Lecture (hours/week)	Seminar (hours/week)	Lab. (hours/week)	Credits	ECTS
CMP 119	A	Fall	3.00	1.00	0.00	3.50	5.00

Lecturer	Artur Koci, PhD
Assistant	Edlir Spaho, MSc
Course language	English
Course level	Bachelor
Description	The internal understanding of modern computer systems and the free trade present in hardware-software interfaces: Guidance placed on the design and handling of modes, registers, internal CPU bus structures, computer arithmetic, memory systems, input-output systems, and the study of real computers and microprocessors.
Objectives	The internal understanding of modern computer systems and the free trade present in hardware-software interfaces: Guidance placed on the design and handling of modes, registers, internal CPU bus structures, computer arithmetic, memory systems, input-output systems, and the study of real computers and microprocessors.
Core Concepts	

Course Outline

Week	Topic
1	Introduction to Computer Organization: This topic covers the generations of digital computers, types of computers, and their classifications. A general description of functional units and their interconnection, types of buses, bus architecture, bus arbitration, and a general description of registers and data transfer between registers and main memory is provided.
2	Digital Logic Circuits: This topic provides a general description of logic circuits. The concept of combinational and sequential logic circuits is given. AND, OR, NAND, XOR gates, and their truth tables are explained.
3	Digital Logic Circuits: This topic gives a brief description of combinational circuits and describes decoder and multiplexer logic circuits along with their truth tables. It also gives a brief description of sequential circuits, including SR, JK, and D Flip-Flop circuits along with their truth tables.
4	Central Processing Unit (CPU): This topic explains the concept of signed binary numbers, addition and subtraction of signed binary numbers, the carry-over and overflow concept, and sign extension. It also covers the organization of the processor, the general organization of registers, and the organization of the stack.
5	Addressing Modes: This topic discusses addressing modes, describing the two main types of addressing: direct addressing and indirect addressing, along with the advantages of each method. Various examples are also provided to illustrate each mode.
6	Assembly Language and Types of Instructions: This topic covers data transfer instructions, data processing instructions, program control instructions, and branch instructions (with condition).
7	Organization of the Central Unit: This topic discusses communication within the central unit, buses, key characteristics of buses, the organization of central unit elements, and the use of specialized logic for address calculation.
8	Midterm Exam

9	Organization of the Central Processing Unit: This topic covers the organization of general-purpose register processors, instruction execution, register transfer, performing arithmetic and logic operations, and multiple bus organization.
10	Pipeline Processors: This topic introduces the basic concepts of pipelining, pipeline performance, the number of pipelining stages, and branch handling.
11	Pipeline Processors: This topic addresses data dependencies, side effects, addressing modes, multiple execution units, and performance analysis.
12	Memory and Its Organization: This topic gives a general description of memory, memory hierarchy, Random Access Memory (RAM), and methods for improving the performance of main memory.
13	Cache Memory and Its Organization: This topic discusses cache memory, the ways it is implemented, its advantages, limitations, and cache block replacement algorithms.
14	Peripheral Subsystem (PS): This topic gives a general description of the peripheral subsystem, its functioning, and the interfacing of peripheral devices.
15	Input/Output Techniques: This topic discusses blocking techniques, status blocking techniques, Direct Memory Access (DMA), and I/O processors.
16	Final Exam

Prerequisites	The student must attend the course at a minimum rate of 75%.
Literature	• Organizimi dhe Arkitektura e Kompjuterave- Agim Cami. Leksione te pergatitura nga pedagogu i lendes.
References	• Carl Hamacher, Zvonko Vranesic, Safëat Zaky and Naraig Manjikian, “Computer Organization and Embedded Systems”, Sixth Edition, McGraë, Hill, 2012. 2. Carl Hamacher, Zvonko Vranesic and Safëat Zaky, “Computer Organization”, Fifth Edition, Tata McGraë, Hill, 2002.

Course Outcome

1	Understand fundamental knowledge of building the central processing unit using digital gate logic.
2	Understand fundamental knowledge of the functioning of the control structure of the central processor.
3	Understand basic knowledge of the I/O system.
4	Understand the micro-architecture of the processor and pipeline technology.
5	Understand memory organization, virtual memory, and cache.
6	Understand the functioning of the input-output mechanism.

Course Evaluation

In-term Studies	Quantity	Percentage
Midterms	1	30
Quizzes	0	0
Projects	1	10
Term Projects	0	0
Laboratory	0	0
Class Participation	1	10
Total in-term evaluation percent		**50**
Final exam percent		**50**
Total		**100**

ECTS Workload (Based on Student Workload)

Activities	Quantity	Duration (hours)	Total (hours)
Course duration (Including the exam week: 16x Total hours of the course)	16	4	64
Study hours outside the classroom (Preparation, Practice, etc.)	14	3	42
Duties	1	0	0
Midterms	1	8	8
Final Exam	1	12	12
Other	1	2	2
Total Work Load			**128**
Total Work Load / 25 (hours)			**5.12**
ECTS			**5.00**